ASML

# Stronger partnerships: Reducing risks, accelerating progress

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# Agenda



- Partnerships 2.0 – Accelerate and de-risk new technologies
- EUV – Progress and update
- Immersion – Double patterning update
- 450 mm update
- Summary and conclusions

# It’s all about trust



$$\text{Trust} = \frac{\text{Capability x Transparency x Reliability}}{\text{Self-Interest}}$$

# Deeper partnerships throughout the value chain



Suppliers


Customers

**Suppliers should understand customer needs**

**Customers should understand supplier capabilities**

**Partnerships drive the right balance**

# Customer Co-Investment Program: Rationale



- Industrialization of EUV Lithography and transition to 450 mm are **essential enablers for Moore's Law** and deliver the required **economic benefits**
- Increasing **complexity** and huge **investments** make it necessary to have **risk sharing** amongst customers and suppliers

**Sharing the risk:**
**Technology funding €1.38B**

**Sharing the reward:**
**Equity participation € 3.85B**

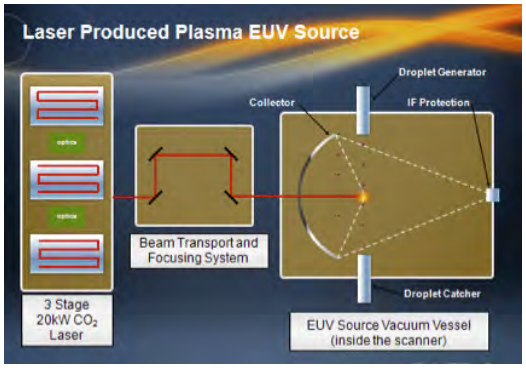
# Acquisition of Cymer



## Merging ASML and Cymer:

- Creates efficiency in EUV technology development
- Accelerates Industrialization of EUV source
- Simplifies EUV source supply chain
- Optimizes manufacturing flow of EUV modules

ASML + CYMER ®



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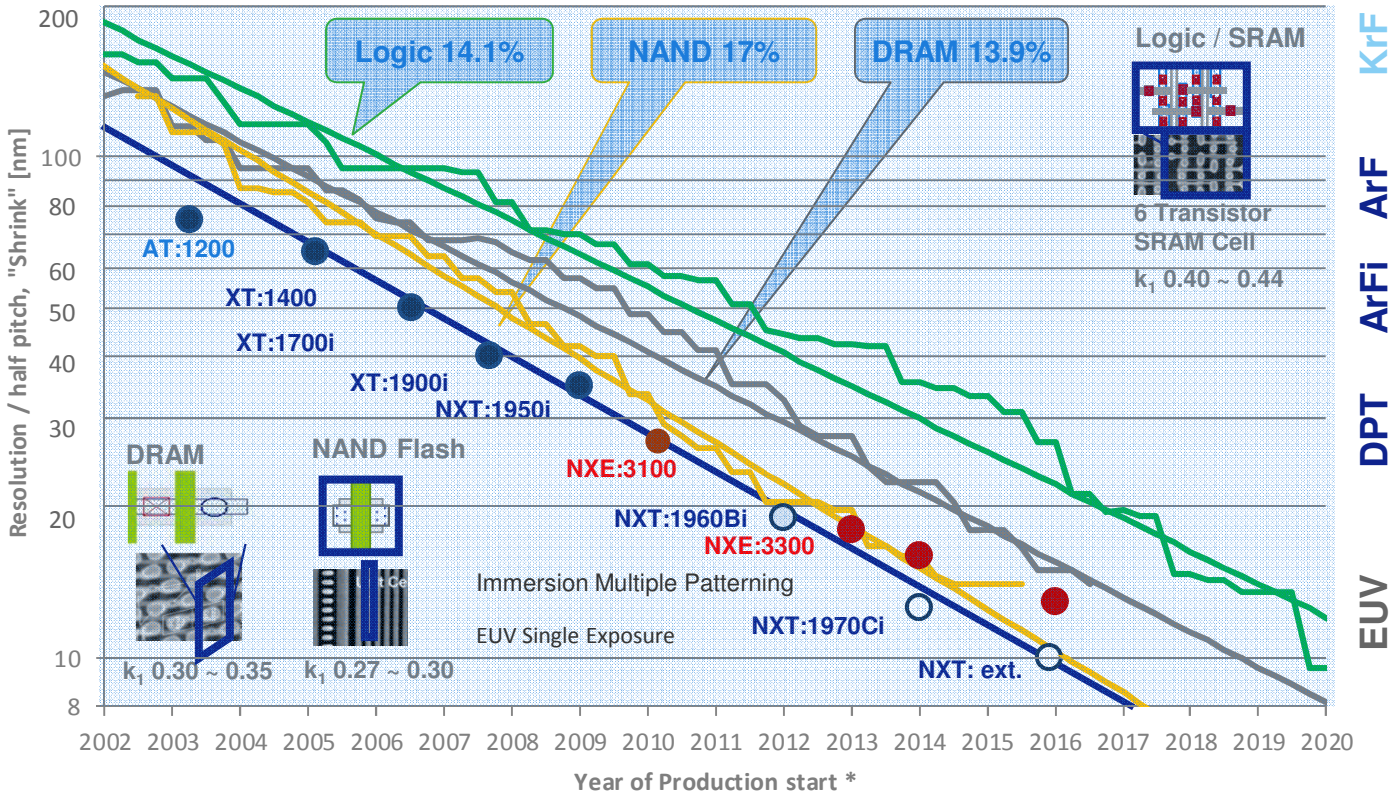
# Industry roadmap towards < 10 nm resolution

## Lithography supports shrink roadmap




* Note: Process development 1.5 ~ 2 years in advance updated Dec/12

# ASML's NXE:3100 and NXE:3300B



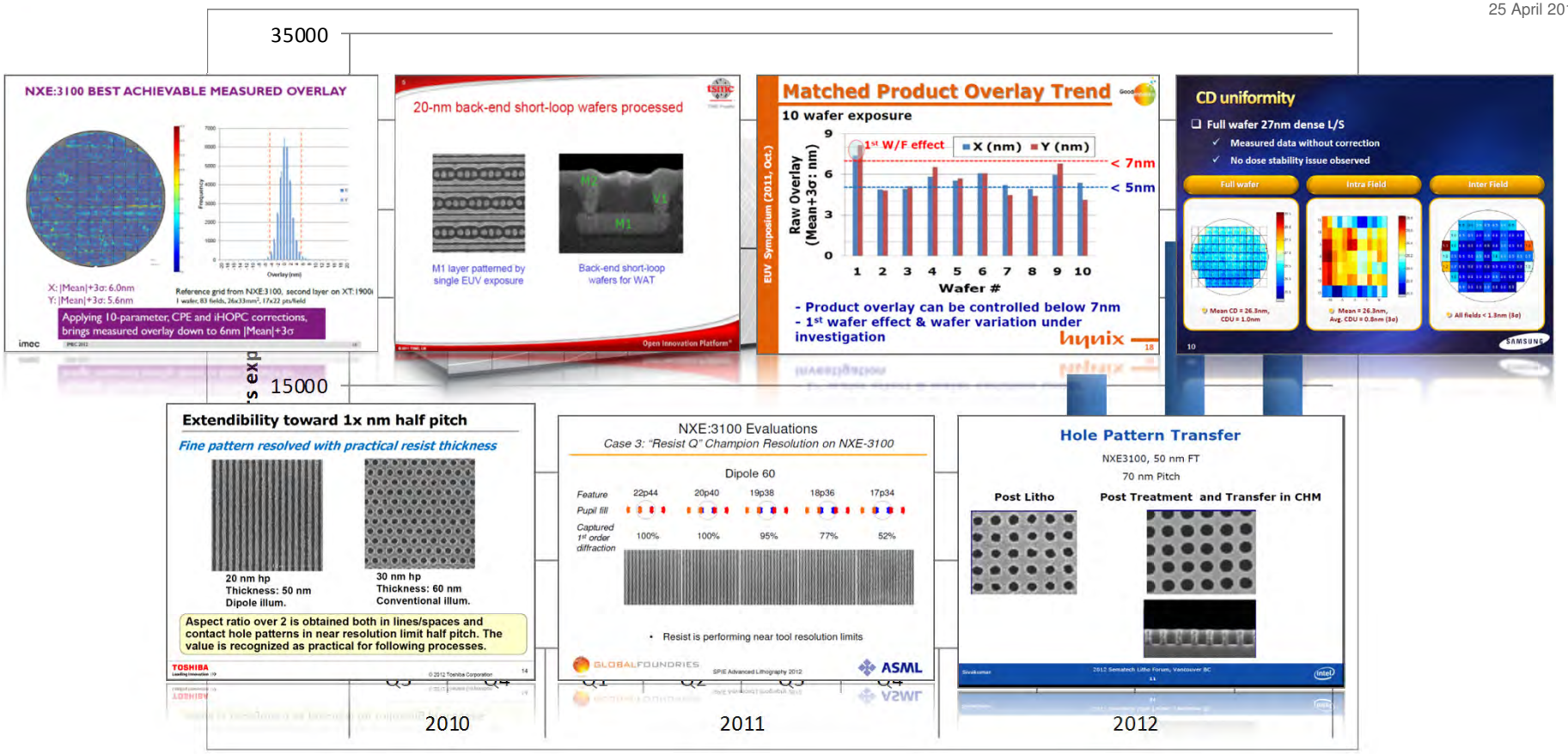


| | NXE:3100 | NXE:3300B |
|---|---|---|
| NA | 0.25 | 0.33 |
| Illumination | Conventional 0.8 σ | Conventional 0.9 σ<br>Off-axis illumination |
| Resolution | 27 nm | 22 nm |
| Dedicated Chuck Overlay / Matched Machine Overlay | 4.0 nm / 7.0 nm | 3.0 nm / 5.0 nm |
| Productivity | 6 - 60 Wafers / hour | 50 - 125 Wafers / hour |
| Resist Dose | 10 mJ / cm2 | 15 mJ / cm2 |

# The **NXE:3100** has exposed >30,000 wafers

*Enabling customers to go through cycles of learning*





# Eleven NXE:3300B systems in various states of integration

*New clean room completely finalized in July 2012*



System 1:

System 2:

Development tool

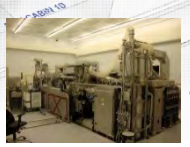
System 7

System 8

System 10
Training

System 3:

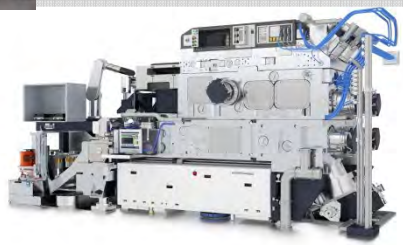
System 5



System 9

System 4

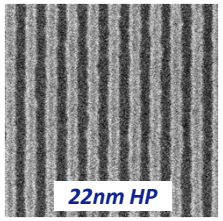
System 6



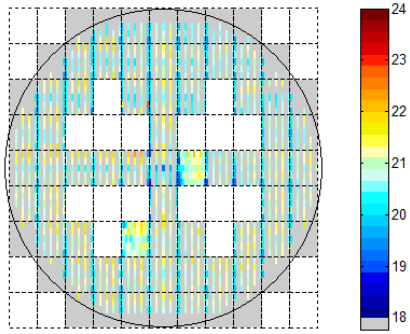
# NXE:3300B imaging and overlay beyond expectations



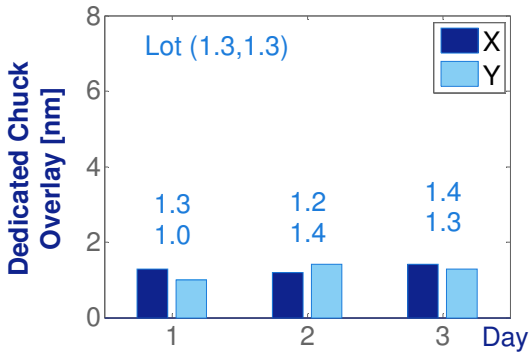
## Scanner qualification

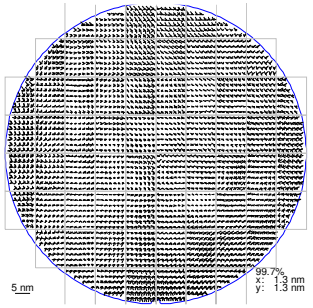



BE = 15.9 mJ/cm²
EL = 13%
DoF = 160 nm

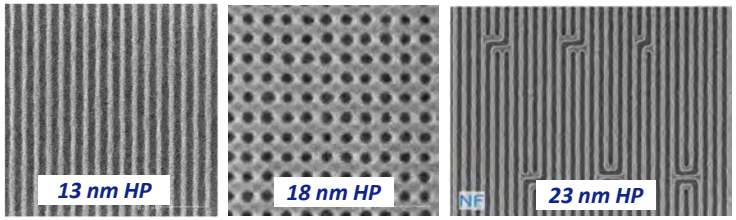


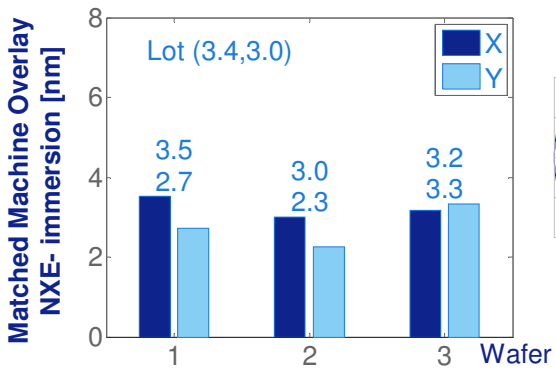

*Full wafer CDU = 1.5nm*

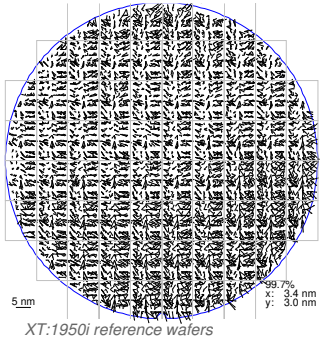



## Scanner capability



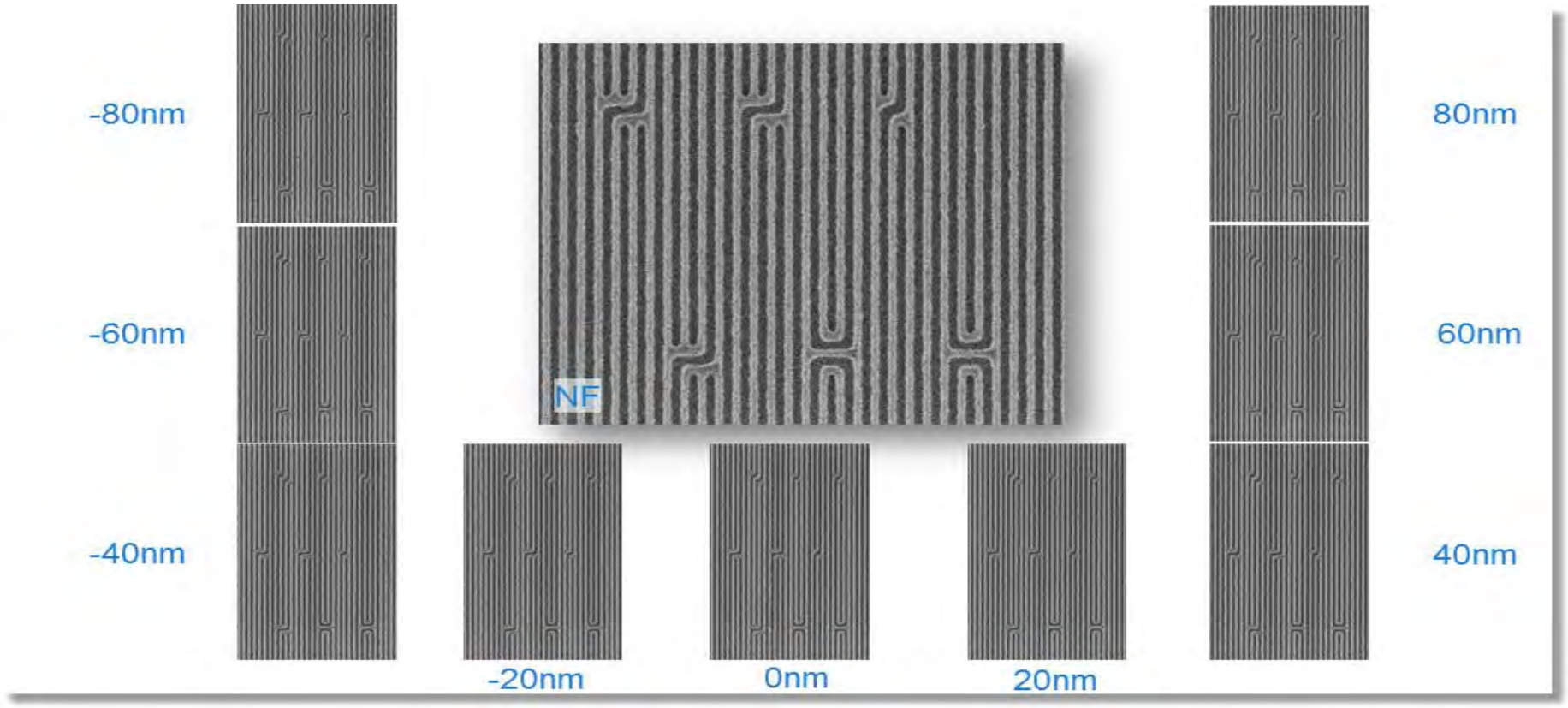




*XT:1950i reference wafers*
*EEXY sub-recipes*
*18par (avg. field) +*
*CPE (6 par per field)*

# NXE:3300B - Good imaging performance logic metal1

*~10 nm logic node, minimum half-pitch 23 nm, single exposure printing*

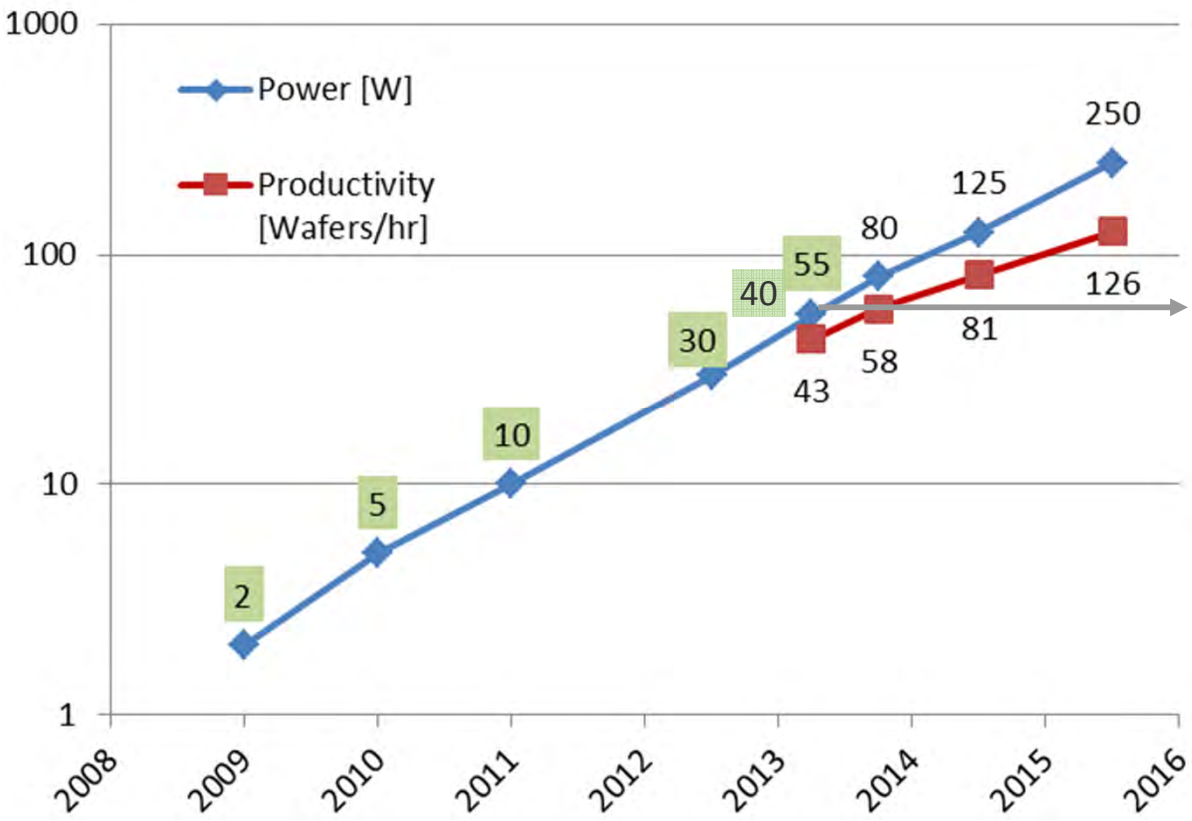


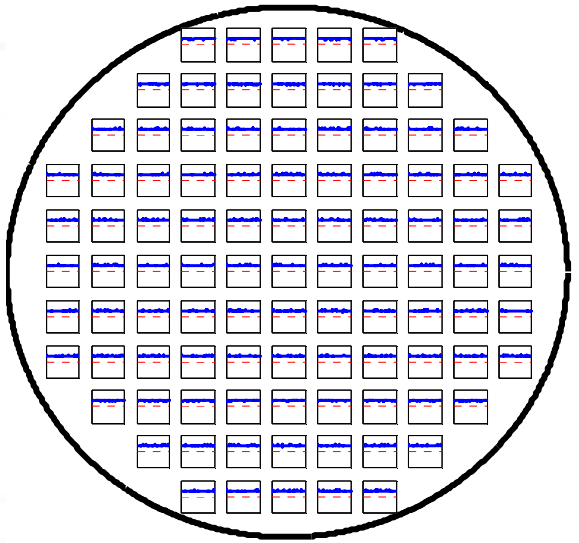


# EUV Source Power Progress reaching 55 W

*Supporting 43 wafers/hour, 250 W target to be reached in 2015*





**At 55 W, 1 run:**
**97.5% of the dies < 0.5% dose**

**At 40 W, 6 runs:**
**99.99 of the dies < 0.2% dose,**

**7 one hour runs total representing**
**~ 250 exposed wafers @ 15 mJ/cm²**

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# ArF immersion for cost-efficient Double and Quadruple Patterning

*NXT platform will be ready for all critical layers*



| Litho Requirements | 2010 – 2012 | 2013 – 2014 | 2014 – 2015 | 2016 – 2018 |
|---|---|---|---|---|
| On Product Overlay | 9 nm | 6 nm | 4 nm | 3 nm |
| CD Uniformity iso | 3 nm | 1.5 nm | 1 nm | <1 nm |
| Total Focus Budget | 100 nm | 80 nm | 60 nm | <60 nm |

| | NXT:1950i | NXT:1960Bi | NXT:1970Ci | NXT Extensions |
|---|---|---|---|---|
| Timing | Q4 2011 | Q1 2013 | Q4 2013 | 2H 2015 |
| DCO / MMO | 2.5 / 5.5 nm | 2.5 / 4.5* nm | 2.0* / 3.5* nm | <1.5* / <2.5* nm |
| Full Wafer Focus Unif | 30 nm | 22 nm | 20 nm | 15 nm |
| Full Wafer CDU (iso) | 3.0 nm | 2.0 nm | 1.3 nm | 1.0 nm |
| Throughput (96 shots) | 190 WpH | 230 WpH | 250 WpH | 250 WpH |
| Defects/Wafer | 10 | 10 | <7 | <7 |

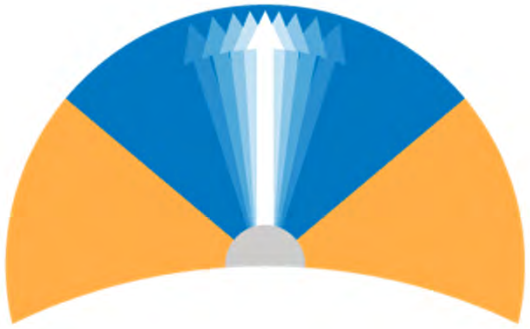
**** Full Wafer to reference***

# Holistic lithography supports shrink roadmap



## Process window enlargement

- OPC / OPC verification
- Illumination / wave front / mask optimization
- Application-specific corrections

## Process window control

- Baseliner + stand alone metrology to maintain scanner stability and matching
- Optimizers + integrated metrology to correct layout and process influences

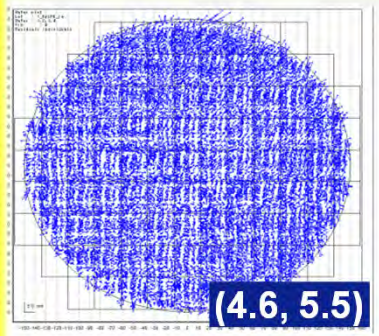
# Integrated Metrology is the only viable way to control volume production for 20 nm process and below

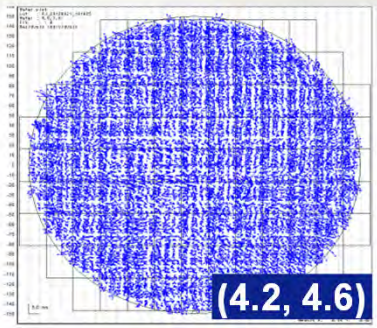
# Integrated Metrology drives on product performance improvements



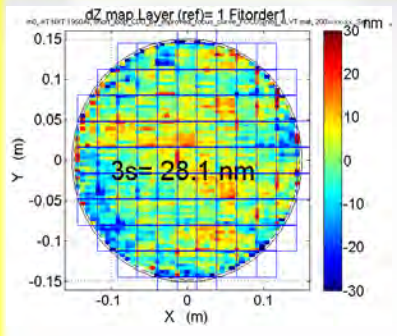

**4 Key technical differentiators:**

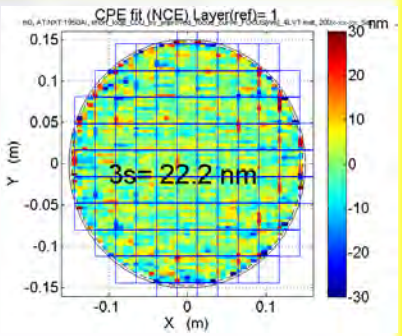
- Integration on Track
- Measurement accuracy with diffraction-based overlay
- Small targets for in die measurements
- Focus measurement with asymmetric targets




0.9 nm OPO improvement measured




30% focus uniformity improvement

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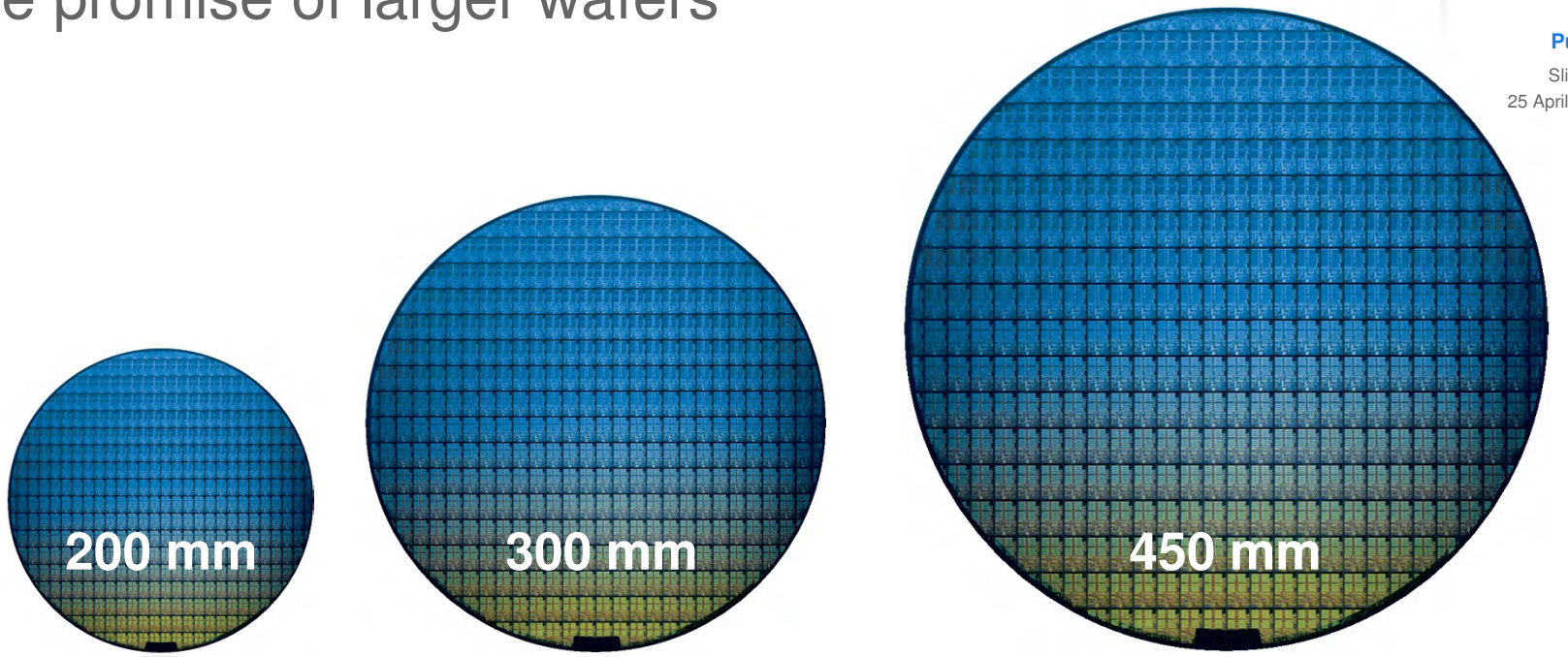
# The promise of larger wafers






| | | |
|---|---|---|
| Wafer Area | 2.25X | 2.25X |
| Effective Area | 2.36X | 2.40X |
| Cost Reduction Goal | 30% | 30% |

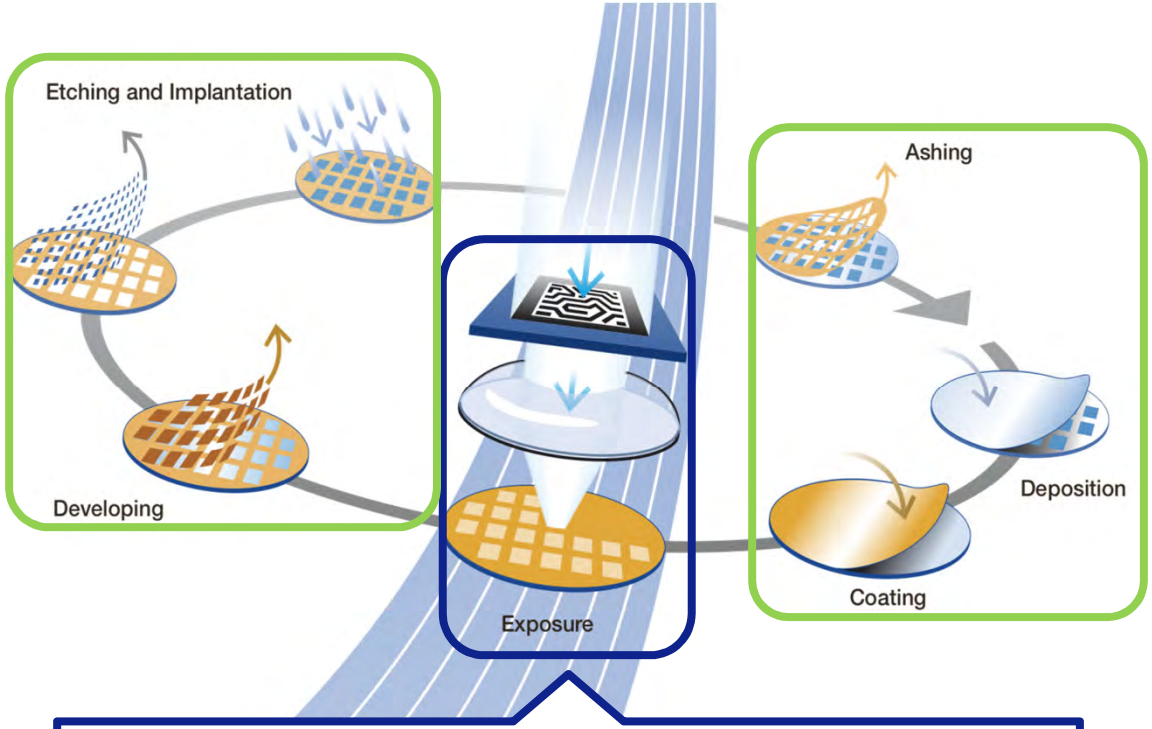
Source: Shang-yi Chiang, tsmc, SPIE March 2011

# Lithography is at the heart of chip manufacturing

*450 mm wafers only provide limited cost benefit for scanning systems*



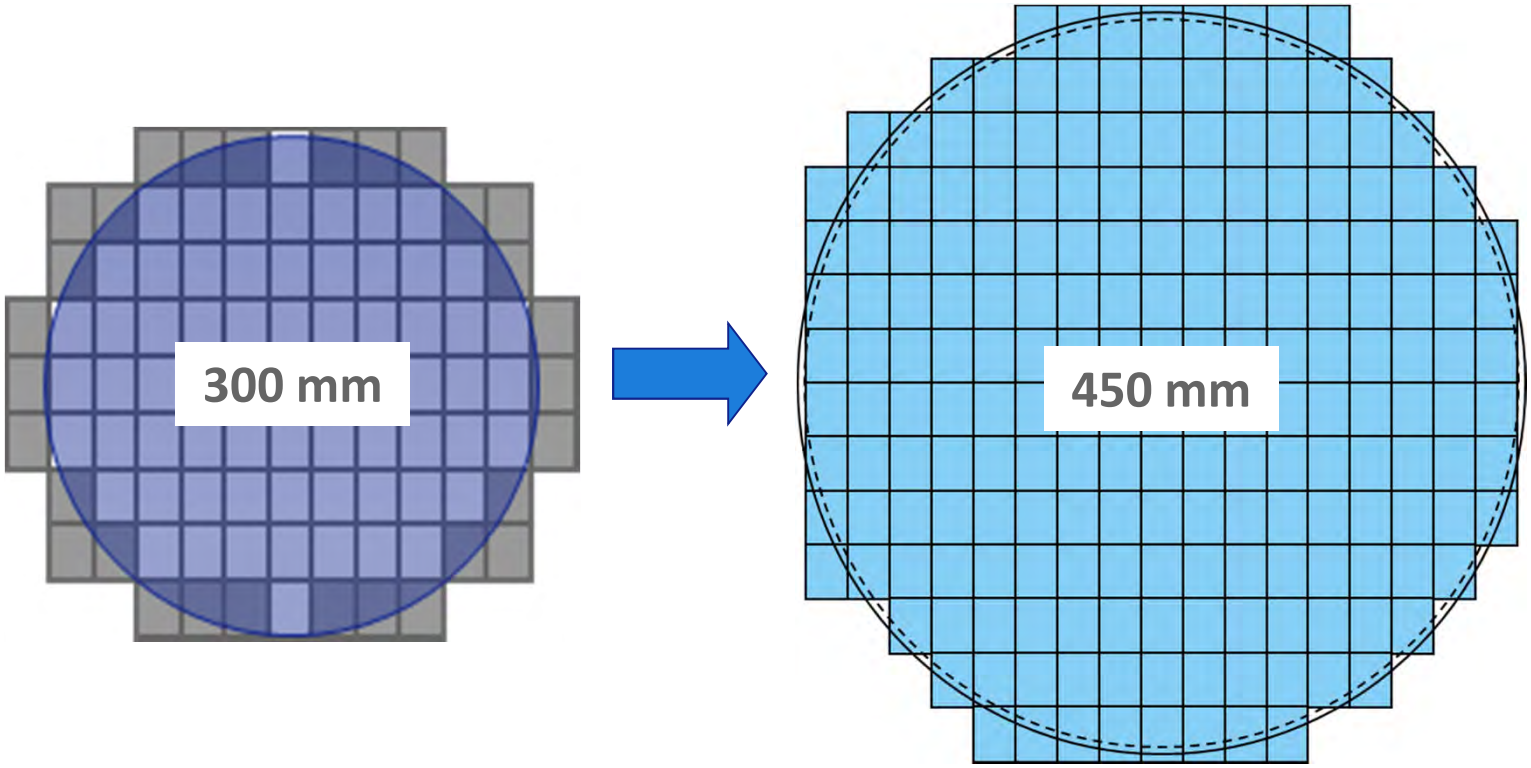
*Non-scanning* process equipment can provide cost advantage from wafer size increase to 450 mm




*Scanning* (lithography) systems provide limited cost benefit from wafer size increase to 450 mm

# Silicon area patterned per hour is comparable for 300 mm and 450 mm lithography tools

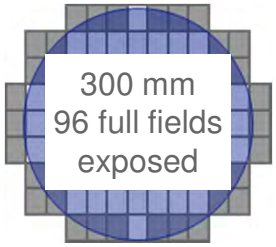
*450 mm wafer throughput is ~50% of 300 mm wafer throughput*

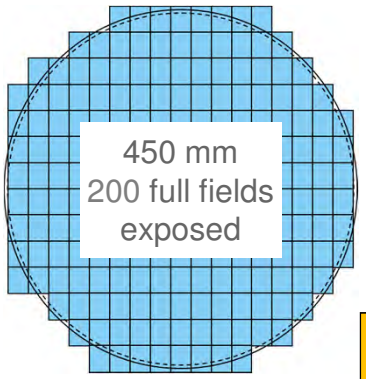


# Litho economics 300 mm => 450 mm challenging

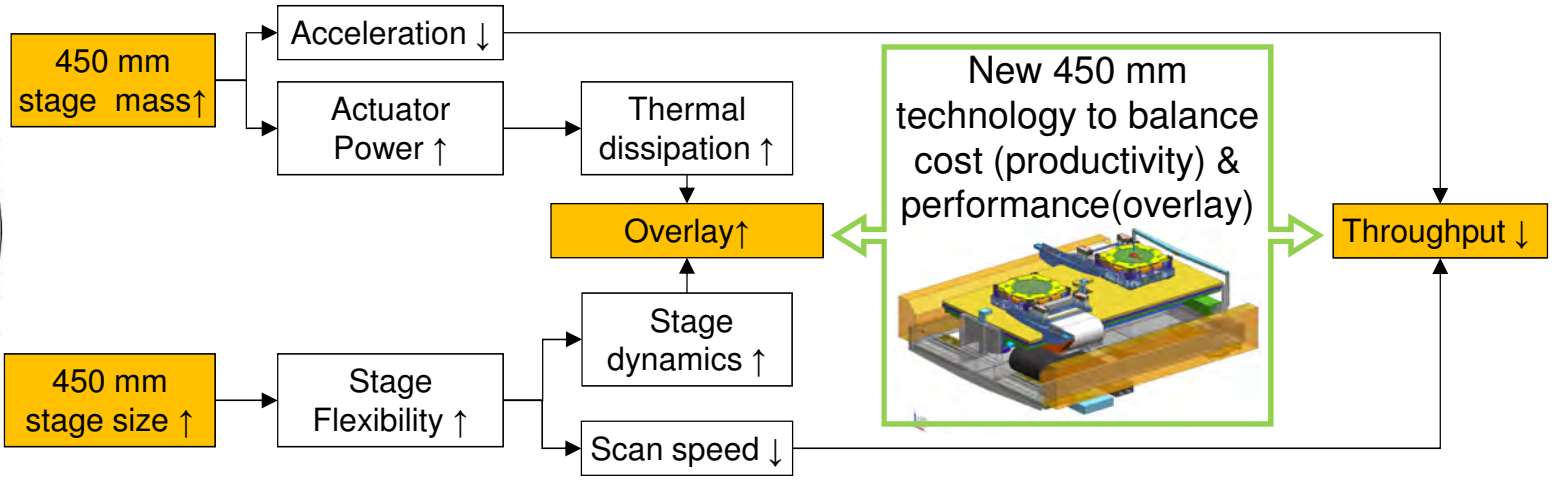
*New technology needed to stay neutral in cost*






| | throughput | | | Relative cost | |
|---|---|---|---|---|---|
| | WpH | m2/H | 450/300 mm | Cost | Cost/ m2 |
| 300 mm limit | 250 | 18 | 1.0 | 1.0 | 100% |
| 450 mm linear stage scaling | 100 | 16 | 0.9 | 1.1 | 122% |
| 450mm new technology | 125 | 20 | 1.1 | 1.1 | 100% |



# 450 mm for productivity and cost



- Customers increasingly concerned about manufacturing cost. ASML will enable continuous cost reduction, primarily through shrink. Shrink becomes a bigger risk for our customers given the overall technology risk. 450 mm looks like a doable cost reduction scenario.
- 450 mm wafers provide limited cost benefit for scanning systems
- Significant enhancements in overlay are required next to wafer size increase to accommodate the roadmap
- ASML has engaged with a funding program over the next 5 years with its major customers to accelerate their development programs including 450 mm
- ASML has initiated 450 mm program on 2 platforms and 4 wavelengths
- Early version tools in 2015/16, volume systems in 2018
- Overall concern remains due to limited overall industry 450 mm implementation plans

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# Affordable shrink roadmap



2012 2013 2014 2015 2016 2017 2018 2019 2020

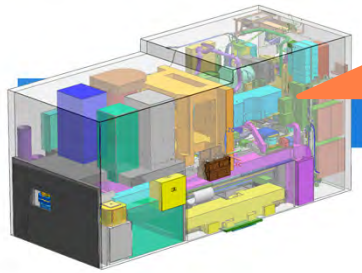
Immersion

**Performance scaling on Immersion litho:**
On Product Overlay (OPO) <8.5 nm ➔ < 3 nm
Critical Dimension Uniformity (CDU) <2.0 nm ➔ 1 nm
Throughput 200 wafers per hour (wph) ➔ >250 wph

EUV

**Economics and extendibility of EUV:**
Resolution 22 nm ➔ 8 nm
EUV to immersion overlay 5.0 nm ➔ 2 nm
Throughput 70 wph ➔ >125 wph

450mm



**Cost opportunity of 450 mm:**
Boost die throughput
No litho cost increase per die

# Summary and Conclusions

- In combination with a holistic approach, immersion technology is capable of supporting shrink to 14 & 10 nm:
  - Optimization of mask, illuminator (FlexRay) and pupil (FlexWave)
  - Integrated Metrology with Yieldstar
- Once power is sufficient for 125 wafers per hour, EUV becomes technology of choice for high volume production of key layers
  - Key resources and stake holders aligned through co-investment program and Cymer acquisition
- Industry aligning on 450 mm insertion point around 10 nm node
  - “EUV first, 450 mm later”
- More / deeper partnerships required throughout the industry to maintain speed and affordability


ASML